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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No	**240703-1170**
First Named Inventor	**Neil Birkett, et al.**
Title	**Complex Filtering/AGC Radio Receiver Architecture for Low-IF or Zero-IF**
Express Mail Label No	**EL492176087US**

APPLICATION ELEMENTS

See *MPEP Chapter 600 concerning utility patent application contents*

1. [+] *Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original, and a duplicate for fee processing)*
2. [ ] Applicant claims small entity status
3. [+] Specification *(preferred arrangement set forth below)* — *[Total Pages* **18** *]*
   - Descriptive title of the invention
   - Cross References to Related Applications
   - Statement Regarding Fed. Sponsored R&D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [+] Drawing(s) *(35 USC d113)* — *[Total Sheets* **6** *]*
5. Oath or Declaration — *[Total Pages* **5** *]*
   a. [+] Newly Executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
6. [ ] Application Data Sheet. See 37 CFR 1.76

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy (CRF)
   b. Specification Sequence Listing on
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] Paper
   c. [ ] Statements verifying identity of above copies

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09/675513
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ACCOMPANYING APPLICATION PARTS

9. [+] Assignment Papers (cover sheet & Documents(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [+] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [+] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other

17. If a **CONTINUING APPLICATION,** *check appropriate box and supply the requisite information below and in a preliminary amendment, OR IN AN Application Data Sheet under 37 CFR 1.76:*

☐Continuation ☐Divisional ☐Continuation-in-part (CIP) of prior application No: /

Prior application information: *Examiner* _____ ***Group / Art Unit:*** _____

For CONTINUATION OR DIVISIONAL APPS only: the entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. This incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. CORRESPONDENCE ADDRESS

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Name (Print/Type)	**Daniel J. Santos**	*Registration No. (Attorney/Agent)*	**40,158**
Signature	Daniel J. Santos	*Date*	9/29/00

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Neil Birkett, et al.

For: Complex Filtering/AGC Radio Receiver Architecture for Low-IF or Zero-IF

CERTIFICATE OF EXPRESS MAIL

Assistant Commissioner for Patents
BOX: Patent Application
Washington, D.C. 20231

Sir:

Enclosed for filing in the above case are the following documents:

Return Postcard
Patent Application (18
Informal Drawings (6)
Executed Declaration & POA
Executed Assignment and Assignment Cover Sheet
Fee Transmittal document
Credit Card Authorization Form

Further, the Commissioner is authorized to charge Deposit Account No. 20-0778 for any additional fees required. The Commissioner is requested to credit any excess fee paid to Deposit Account No. 20-0778.

Respectfully submitted,

Daniel J. Santos; Reg. No. 40,158

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
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Atlanta, Georgia 30339-5948

Our Docket No: **240703-1170**

I hereby certify that all correspondences listed above are being deposited for delivery to the above addressee, with the United States Postal Service **"EXPRESS MAIL POST OFFICE TO ADDRESSEE"** service under 37 CFR §1.10 on the date indicated below:

The envelope has been given U.S. Postal Service "Express Mail Post Office To Addressee" Package # **EL492178087US**.

Date: 9.29.00

Allison M. Olson

FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1
These are the fees effective December 29, 1999
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12

TOTAL AMOUNT OF PAYMENT ($) 748.00

Complete if Known	
Application Number	TBD
Filing Date	TBD
First Named Inventor	BIRKETT, et al.
Examiner Name	TBD
Group / Art Unit	TBD
Attorney Docket No.	240703-1170

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge to the following Deposit Account.

Deposit Account Number: 20-0778

Deposit Account Name: Thomas, Kayden, Horstemeyer Risley

☒ Charge any additional fee required and requested to credit any overpayment ☐ Charge all indicated fees and any additional fee required or credit any overpayment

2. ☐ **Payment Enclosed:**

☐ Check ☐ Money Order ☒ Credit Card

FEE CALCULATION

1. BASIC FILING FEE

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	$690
106	310	206	155	Design filing fee	$
107	480	207	240	Plant filing fee	$
108	760	208	380	Reissue filing fee	$
114	150	214	75	Provisional filing fee	$
				SUBTOTAL (1)	($)690

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	21	-20**=	1	x	18.00	=	18
Independent Claims	1	-3** =	0	x	78.00	=	0
Multiple Dependent					260.00	=	0

**or number previously paid, if greater, For Reissue, see below

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent Claims in excess of 3
104	260	204	130	Multiple dependent claims in excess of 3
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent
				SUBTOTAL (2) ($)18

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	380	216	190	Extension of time within second month	
117	870	217	435	Extension of time within third month	
118	1,360	218	680	Extension of time within fourth month	
128	1,850	228	925	Extension of time within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (time number of properties)	
146	760	246	380	Filing a submission after final rejection (37 CFR 1.129(a))	
149	760	249	380	For each additional invention to be examined (37 CFR 1.129(b))	
				Other fee (specify) Assignment Recordation Fee	40.00
				Other fee (specify)	
				*Reduced by Basic Filing Fee Paid SUBTOTAL (3)	40.00

SUBMITTED BY		Complete (if applicable)	
Typed or Printed Name	DANIEL J. SANTOS	Reg. Number	40,158
Signature	Daniel J. Santos	Date 9/29/00	Deposit Account User ID

Complex Filtering/AGC Radio Receiver Architecture for Low-IF or Zero-IF

Field of the Invention

The invention relates generally to circuitry for filtering and amplifying signals, and more particularly to a complex Filtering/Automatic Gain Control architecture for zero-IF or low-IF radio receivers.

Background of the Invention

Present day RF radio receivers must be capable of detecting and demodulating RF signals in which the desired information signal is often much weaker than existing interfering signal. Recently, receivers which directly convert the RF signal to a much lower frequency have been developed. The RF signal is down-converted to a zero-IF or low-IF intermediate frequency where analog and/or digital signal processing is more efficient. Present day radio receivers typically employ real filters to filter out interfering signals, and amplifiers to increase the level of the desired signal. If real filters are used in a LIF path they have the disadvantage of not differentiating between negative frequencies and positive frequencies, hence a high performance image reject mixer is typically used to separate the positive/negative frequencies. In addition, where the frequency of the interfering signal is close to the frequency of the desired signal in a LIF architecture, a substantial number of filter poles are required to filter out the interfering signals and the overall amplifier circuit is such that considerable power is required to amplify the desired signal to an appropriate level for demodulation. In addition, DC offsets caused by both circuit imperfections and characteristics inherent in certain forms of modulation must be removed since they can be several orders of magnitude larger than the desired signal and can degrade the performance of the final demodulator circuit.

Therefore, there is a need for a simpler architecture for enhancing the gain performance and removing DC offsets while minimizing power consumption.

Summary of the Invention

The invention is directed to apparatus for filtering and amplifying a received signal. The apparatus includes a plurality of complex filter/amplifier stages connected in sequence. Each of the stages has a complex filter for attenuating an interfering portion of the received signal relative to the desired portion, a controlled amplifier which has set minimum gain K_{min} and maximum gain K_{max} for amplifying the received signal, where K_{min} may be negative, and a control circuit. The control circuit controls the amplifier gain K where $K_{min} \leq K \leq K_{max}$ such that the controlled amplifier seeks to generate an output signal having a projected amplitude level. The present invention is particularly advantageous in that the apparatus is capable of providing an overall output signal at a predetermined amplitude level within a restricted dynamic range from input signals having a wide variety of signal strengths and at the same time permits for the use of low power consuming subsequent circuits. This is achieved in apparatus that itself draws very low power. The apparatus operates effectively on received signals in the IF band that are low-IF or zero-IF

In accordance with another aspect of this invention, the received signal is made up of complex in-phase I and quadrature phase Q signals. The complex filter may be multipolar or may be one or more single pole complex filters connected in series. The controlled amplifier has a first variable gain amplifier for amplifying the in-phase I signal and a second variable gain amplifier for amplifying the quadrature phase Q signal. The control circuit generates a gain control signal which is a function of the outputs or the inputs of the amplifiers as well as a function of a projected amplitude level.

In accordance with a further aspect of this invention, the control circuit may include a first and a second rectifier for receiving the inputs of the first and second variable amplifiers respectively or the outputs of the first and second variable amplifiers respectively to provide first and second rectified signals. The rectified signals are added in a summing circuit and fed to an error amplifier where the summed signal is compared to a projected amplitude level signal for producing the gain control signal used to control the gain of the amplifiers.

With regard to another aspect of this invention, the apparatus may further include a received signal strength indicator which has a gain summation circuit for receiving the gain control signal from each of the complex filter/amplifier stages to compute the overall gain of the apparatus and a detector to detect the amplitude of the apparatus overall output signal for determining the strength of a desired signal received by the apparatus.

Other aspects and advantages of the invention, as well as the structure and operation of various embodiments of the invention, will become apparent to those ordinarily skilled in the art upon review of the following description of the invention in conjunction with the accompanying drawings.

Brief Description of the Drawings

The invention will be described with reference to the accompanying drawings, wherein:

Figure 1 schematically illustrates the invention;

Figure 2 illustrates an embodiment of the present invention;

Figure 3 illustrates a complex single pole filter which may be used with the present invention;

Figure 4a illustrates a quadrature feedback AGC circuit in accordance with the present invention having DC feedback compensation;

Figure 4b illustrates a quadrature feedback AGC circuit in accordance with the present invention having DC feedforward compensation;

Figure 5a illustrates a quadrature feedforward AGC circuit in accordance with the present invention having DC feedback compensation;

Figure 5b illustrates a quadrature feedforward AGC circuit in accordance with the present invention having DC feedforward compensation; and

Figure 6 illustrates a control circuit for the AGC's in accordance with the present invention.

Detailed Description of the Invention

Though the present invention is described in conjunction with figure 1 within the environment of an RF radio receiver, it may also be used in other applications where circuitry that has very low power consumption levels is required. An RF radio receiver 10 includes, at its front end, an RF/IF down converter 11 for converting the input RF signal to low-IF (LIF) or zero-IF (ZIF) in-phase I_i and quadrature Q_i signals. The RF radio receiver further includes a digital demodulator 12 at its back end for digitizing the amplified in-phase I_o and quadrature Q_o signals and demodulating the digitized signals to provide at its output the data from the input RF signal. In most circumstances, the quadrature I_i and Q_i signals cannot be applied directly to the digital demodulator 12. The desired signal, whether it is too small or too great for the demodulator 12 is embedded in an interfering signal. The desired signal is usually very small relative to the interfering signal, the interfering signal being as high as 60 db greater than the desired signal. In order to be able to detect and demodulate the desired signal portion of the input signal, the amplitude of the desired signal must be made greater than the interfering signal, and the amplitude of the desired signal must also be at a level that can be efficiently digitized and demodulated, this is carried out by passing the input signals through bandpass filters and amplifiers.

Figure 1 schematically illustrates a novel cascaded structure 13, in accordance with the present invention, for filtering and amplifying the in-phase I_i and quadrature Q_i input signals to produce in-phase I_o and quadrature Q_o output signals having which can be efficiently digitized and demodulated. In order to be able to use an efficient analog to digital converter (ADC), it is advantageous that the overall in-phase I_o and quadrature

Q_o output signals be produced at a predetermined level H within a restricted dynamic range whether the desired portion of the input signal is initially far below or even above the predetermined level H. The more restricted the dynamic range, the smaller the number of bits required in an ADC to digitize the signal, this reduces the power requirements for the ADC.

The cascaded structure 13 includes a series of complex filter/amplifier stages 14_1, 14_2, ... 14_n which each in turn independently filter and amplify the complex signal until the desired portion of the complex signal achieves a predetermined amplitude level H that falls within the desired restricted dynamic range and is relatively greater than the interfering signal. Though the stages 14_1, 14_2, ... 14_n are described in terms of a filter/amplifier sequence of components, it is understood that the sequence of components could equally be amplifier/filter in all embodiments of the present invention. The filter in each stage 14_1, 14_2, ... 14_n may be a single or multiple pole filter and the amplifiers in stages 14_1, 14_2, ... 14_n are amplitude gain controlled amplifiers which each exhibit an individual gain range having a minimum gain which may be positive or negative and a maximum positive gain. The attenuation of the interfering signal by the filters relative to the desired signal may be distributed equally or unequally over the stages 14_1, 14_2, ... 14_n and the gain range for each stage 14_1, 14_2, ... 14_n may also differ from stage to stage. In addition, AGC settings 15_1, 15_2, ... 15_n are applied to the amplifiers in stages 14_1, 14_2, ... 14_n respectively to control the gain of each amplifier such that the amplitude of the signal at the output of each respective amplifier will tend towards a projected signal level as fixed by the respective AGC setting 15_1, 15_2, ... 15_n. It may occur that one or more amplifiers are driven to operate at its minimum or maximum gain without achieving the projected output signal level called for by AGC setting 15_1, 15_2, ... 15_n at the particular amplifier in that stage.

In operation, the complex filter/amplifier stages 14_1, 14_2, ... 14_n act independently of one another and the stages act sequentially on the input signal so as to produce a desired output signal having a predetermined signal level H falling within the restricted dynamic range required at the output. The signal level H is achieved in the last

stage 14_n by controlling the amplifier within the stage 14_n by the AGC setting 15_n. The AGC setting 15_1, 15_2, ... 15_n are preset at specific levels and represent the projected amplitude level desired at the output of the respective amplifiers. AGC setting 15_1, 15_2, ... 15_n are used to control the gain of the respective amplifiers within their respective gain ranges. The number of stages 14_1, 14_2, ... 14_n in the cascaded structure 13 and the maximum of the gain range for each amplifier is preset in order to obtain the total gain required over the entire cascaded structure 13 to accommodate the variety of desired input signals levels with which the receiver is expected to function properly. The gain ranges or the gain range maximums may be substantially the same, however this will not usually be the case. Each amplifier gain range is preferably selected such that the amplifiers will operate efficiently minimizing power consumption.

Initially, at the input to the RF radio receiver, the desired input signal is relatively much smaller than the interfering signals. Each stage 14_1, 14_2, ... 14_n attenuates the interference signals using a complex filter having one or more poles. The signal is then amplified by an AGC which amplifies both the desired signal as well as the interfering signal. As the signal passes through subsequent stages, the desired signal becomes larger relative to the interfering signal since both are amplified but only the interfering signal is attenuated by the filter. Thus, in the last stages, the desired signal becomes the dominant signal since the interfering signal is being attenuated to towards zero.

As an example, a five stage filter/amplifier structure 13 may have gain ranges for the five stages 14_1, 14_2, ... 14_5, of +5 to -5, +5 to -5, +20 to -5, +20 to -5, and +15 to -5 respectively in order to accommodate the range of signals that it is to detect.

In one scenario, it might be found that a five stage structure 13 is required to detect a desired signal that is 50 db below the level H required for it to be digitized and also about 40 db below the interfering signal. In such a case, the AGC setting 15_1, 15_2 will place a gain demand on the first two stages that are very low, say in the order of 2 and 6 db since the interfering signal is high, such that the filters attenuate the interfering signals significantly while the signals are not being amplified significantly by the

amplifiers in these early stages. At the third stage, with desired signal and the interfering signal being relatively equal, the AGC setting 15_3 may be set at a level which demands a gain of the amplifier greater than its gain range maximum of 20 db. Thus at this stage the amplifier signal gain will be its maximum while its output is lower than that requested. The fourth stage may again have a high AGC setting 15_4, which may demand a gain in the order of 14 db which would be below its maximum of 20 db. Going into the final stage, the AGC setting 15_5 will be set to achieve the desired amplifier output level H. Since the overall gain of the desired signal is the sum of the individual gains, it would be 42 db to this point, and the gain demand on the last amplifier will be 8 db which is below its maximum of 15 db.

In a second scenario taken at the other extreme of possible input signals for the same five stage structure 13, the desired input signal may already be greater than level H required for it to be digitized say for instance about 6db, and at the same time somewhat smaller than the interfering signal. In such a case, the AGC settings 15_1, 15_2 will demand large negative gains of the amplifiers in the first two stages 14_1, 14_2, to get the signal level down. However since the amplifiers have a lower limit of -5db for instance, both the desired signal and the interfering signals will be attenuated by the amplifiers to that limit while the interfering signals will also be attenuated by the filters. It will now be found that the desired signal is below the required output level H by about 4db. In the third to fifth stages 14_3, 14_4 and 14_5, the gain demanded by the AGC settings 15_3, 15_4, and15_5 will be small since the desired signal is only 4 db below the required output level.

One embodiment of the complex filtering/AGC IF architecture in accordance with the present invention is illustrated in figure 2 as part of an RF radio receiver 20. The front end of the receiver 20 includes a quadrature down converter 21 having a pair of mixers 22 and 23 to which the input RF is applied. A synthetic local oscillator 24 with the phase splitter 25 provides second input signals that are at a predetermined frequency, but 90°out of phase, to the mixers 22 and 23 in order to generate quadrature I and Q signals at a low or zero intermediated frequency (LIF or ZIF).

The complex filter/amplifier apparatus 26 comprises a plurality of filter/amplifier stages $27_1, 27_2, \ldots 27_n$ connected in series such that the output of one stage is the input for the next stage. Each stage $27_1, 27_2, \ldots 27_n$ includes a complex filter $28_1, 28_2, \ldots 28_n$ which may have one or more poles as well as an automatic gain controlled amplifier (AGC) $29_1, 29_2, \ldots 29_n$. The AGC's $29_1, 29_2, \ldots 29_n$ are each fed a level control voltage termed the AGC settings $30_1, 30_2, \ldots 30_n$. Though each stage $27_1, 27_2, \ldots 27_n$ is shown to include a complex filter $28_1, 28_2, \ldots 28_n$ followed by an AGC $29_1, 29_2, \ldots 29_n$, the order of these components may be reversed in each stage $27_1, 27_2, \ldots 27_n$.

The output of the last stage 27_n is fed through two analog to digital converters (ADC) 33, 34 and a quadrature detector 39 or digital demodulator which provides the data from the original input data signal.

In addition, a signal representing the actual gains $31_1, 31_2, \ldots 31_n$ of each AGC $29_1, 29_2, \ldots 29_n$ is directed to a received signal strength indicator (RSSI) 32 in order to determine the actual input data signal strength. The input data signal strength is estimated by the RSSI 32 from the sum of the actual gains $31_1, 31_2, \ldots 31_n$ which provides the overall gain of the complex filter/amplifier apparatus 26 and the measured signal level H at the output of stage 27_n. When the gains $31_1, 31_2, \ldots 31_n$ of the AGC's $29_1, 29_2, \ldots 29_n$ are controlled to provide an output signal from stage 27_n that has a relatively constant signal level H regardless of the desired signal level at the input of stage 27_1, then the signal level H is known to be relatively constant and need not be measured to determine the input data signal strength. The received signal strength indicator 32 output is normally used to trigger the processing of a received signal by the radio receiver. However, its other applications could include notifying the base station that its signal requires boosting for the proper operation of the radio system.

An embodiment of a complex filter $28_1, 28_2, \ldots 28_n$ is illustrated in figure 3. The complex filter 35 includes a channel 36_I for the in-phase input I and a channel 36_Q for the quadrature phase input Q. Included in channels 36_I and 36_Q are adders 37_I and 37_Q and integrators 38_I and 38_Q respectively. In addition to the in-phase signal I and quadrature

signal Q being applied to the adders 36_I and 36_Q respectively, a feedback with coefficient α which may be any real number is applied to each adder 36_I and 36_Q respectively. As well, a feedback with negative coefficient β is applied from the output of integrator 38_Q to adder 36_I while a feedback with positive coefficient β is applied from the output of integrator 38_I to adder 36_Q. Coefficient β may also be any real number. The selection of α, β and ω_o will determine the bandwidth and centre frequency of the filter 35. Also, depending on the values of α, β and ω_o the positive and negative frequencies will experience different attenuations which is desired for an LIF device.

Complex filters are particularly advantageous since α, β and ω_o may be varied to vary the centre frequency of the filter while the width of the bandpass about the varied centre frequency can remain the same without changing the number of poles in the filter. As a result, a programmable IF receiver can be designed to switch between IF frequencies.

For a ZIF device, coefficient β goes to 0 as the frequency goes to zero and the cross-coupled coefficients β thus have no effect. In complex filters, the number of poles required to attenuate a signal at a frequency of x Hz away from the centre frequency is independent of the centre frequency while in real filters, the number of poles required to attenuate a signal at a frequency of x Hz away from the centre frequency is dependent on the centre frequency and will always be greater then that required using complex filters except in the case where the centre frequency is zero in which case it is a real filter.

Multipolar complex filters having two or more poles may comprise two or more filters of the type described with reference to figure 3 connected in series.

Embodiments of the AGC's 29_1, 29_2, ... 29_n are illustrated in figures 4a, 4b, 5a and 5b. Fast quadrature feedback AGC circuits using differential signalling will be described with reference to figures 4a and 4b and fast quadrature feedforward AGC circuits using differential signalling will be described with reference to figure 5a and 5b.

The feedback AGC 40 illustrated in figure 4a comprises a pair of channels 41_I and 41_Q for the in-phase signal I and the quadrature signal Q respectively. Adders 42_I and 42_Q and variable gain amplifiers 43_I and 43_Q are connected in series in channels 41_I and 41_Q respectively. The in-phase signal I is applied to one input of the adder 42_I, while the quadrature phase signal Q is applied to one input of adder 42_Q. The gain of VGA's 43_I and 43_Q is controlled by a control circuit 44 which has inputs connected to the outputs of VGA's 43_I and 43_Q to detect the amplitude level of these signals and which has a further input connected to a level setting signal 45 to determine the projected signal levels at the output of the VGA's 43_I and 43_Q. The control circuit 44 output is connected to the VGA's 43_I and 43_Q to control their gains as a function of the difference between the actual and the projected output amplitude levels. The gain may be positive or negative depending on whether the actual signal level is lower or higher respectively than the projected signal level. In addition, the amplifier gain variability is limited to a narrow range which may prevent the signal from being amplified to the projected signal level, but also prevents distortion in low power consumption amplifiers. VGA's 43_I and 43_Q may be linearly or digitally programmable. Digitally programmable VGA's generally consume less power and are therefore preferred.

The feedforward AGC 50 illustrated in figure 5a comprises a pair of channels 51_I and 51_Q for the in-phase signal I and the quadrature signal Q respectively. Adders 52_I and 52_Q and variable gain amplifiers 53_I and 53_Q are connected in series in channels 51_I and 51_Q respectively. The in-phase signal I is applied to one input of the adder 52_I, while the quadrature phase signal Q is applied to one input of adder 52_Q. The gain of VGA's 53_I and 53_Q is controlled by a control circuit 54 which has inputs connected to outputs of adders 52_I and 52_Q to detect the amplitude level of the input signals to VGA's 53_I and 53_Q and which has a further input connected to a level setting signal 55 to determine the projected signal level at the output of the VGA's 53_I and 53_Q. The control circuit 54 output is connected to the VGA's 53_I and 53_Q to control their gains as a function of the difference between the actual input and the projected output amplitude levels. The gain may be positive or negative depending on whether the actual signal level is lower or higher respectively than the projected signal level. In addition, the amplifier gain

variability is limited to a narrow range which may prevent the signal from being amplified to the projected signal level, but also prevents distortion in low power consumption amplifiers. Once again, VGA's 53_I and 53_Q may be linearly or digitally programmable. Digitally programmable VGA's generally consume less power and are therefore preferred.

In addition, CD compensation circuits may be added to the VGA's in order to remove the dc offset. This may done either by using a feedback circuit as illustrated in figures 4a and5a or by using a feedforward circuit as illustrated in figures 4b and 5b.

The feedback DC compensation circuits 46_I and 46_Q in figure 4a detect the dc output of VGA's 43_I and 43_Q and feed back a negative voltage to adders 42_I and 42_Q in order to remove the dc offset on the input signal before the controller 44 estimates the input signal ac levels. The DC compensation circuits 56_I and 56_Q in figure 5a detect the dc output of VGA's 53_I and 53_Q and feed back a negative voltage to adders 52_I and 52_Q in order to remove the dc offset on the input signal before the controller 54 estimates the input signal ac levels. Using the above feedforward control circuit 54, the inclusion of DC feedback will not make the AGC circuit unstable since the dc gain will always be less than unity.

The feedforward DC compensation circuits 47_I and 47_Q in figure 4b detect the dc output of VGA's 43_I and 43_Q and feed forward a negative voltage to adders 48_I and 48_Q in order to remove the dc offset on the output signal before it goes to the next stage in the cascaded structure. Similarly, the feedforward DC compensation circuits 57_I and 57_Q in figure 5b detect the dc output of VGA's 53_I and 53_Q and feeds forward a negative voltage to adders 58_I and 58_Q in order to remove the dc offset on the output signal before it goes to the next stage in the cascaded structure.

In most circumstances, DC compensation circuits 46_I - 46_Q, 56_I - 56_Q, 47_I - 47_Q and 57_I and 57_Q are not required since the filters 28_1, 28_2, ... 28_n will filter out the dc. In particular, complex filters will attenuate all signals whether unwanted ac or dc. However, since the dc offsets may differ in the I and Q signals, performance may be improved by removing the respective dc offsets by DC compensation circuits. In this manner, the dc offsets will not be amplified limiting the range of the VGA's for the wanted signals. In addition, DC compensation is particularly important for ZIF since the filters do not attenuate the dc offsets.

An embodiment of a control circuit 60 which may be used as the control circuit 44, 54 in the embodiments in figures 4a, 4b, 5a, and 5b, is illustrated in figure 6. The control circuit 60 in any filtering/AGC stage detects the magnitude of the ac portion of the amplifier input I and Q signals and sets the required gain for that stage. It is important to accurately detect the magnitude of the ac signal and to quickly make the estimate of the magnitude. In this particular embodiment, the in-phase signal I in channel 61_I and the quadrature signal Q in channel 61_Q are fed to two full wave rectifiers 62_I and 62_Q respectively providing output signals a and b. Signals a and b are added together in an adder 63 to provide an output c having four amplitude peaks per cycle. This rectifying and summing process provides a greater signal amplitude and a faster peak rise time than would be provided by half wave rectifiers. Since many integrated circuits use differential signalling where the amplifiers are differential amplifiers, it is common to have available in these circuits the in-phase $\overline{I}$ signal and the quadrature signal $\overline{Q}$ phase together with the in-phase I signal and the quadrature phase Q signal. Half -wave rectifying each of the four signals above and summing them would provide the same result as full wave rectifying the I and Q signals.

The signal c is then fed to an integrator 64 which smooths the peaks and holds the summed signal c basically acting as a low pass filter to provide the signal d. Signal d is applied to an error amplifier 65 where it is compared to an AGC projected level signal e to provide the required gain estimate output K which is proportional to the difference

between e and d, when e is greater than d. When d is greater than e, then K is negative. In addition, the error amplifier 65 will provide an output signal K which is limited to the predetermined gain range between K_{max} and K_{min} of the AGC in the particular stage that it is operating. Thus $K_{min} \leq K \leq K_{max}$ where K_{min} may be negative. Referring to figure 2, the specific signal K in each particular stage 27_1, 27_2, ... 27_n is used to the control the I and Q VGA's in that particular stage as well as to provide the gain signals 31_1, 31_2, ... 31_n to the RSSI 32.

If the VGA's are linearly controlled and analog in nature, then the error amplifier 65 may be constructed using an analog circuit such as an op-amp whereby both the inputs and outputs are analog. However, if the VGA's are digitally controlled, then the error amplifier 65 may be constructed using digital logic, with inputs and outputs being digital in nature.

The overall advantage of the present invention is that it provides a stable filtering/amplifier structure which minimizes power consumption. Since it is capable of providing desired output signals having an amplitude level within a restricted dynamic range, further power savings may be achieved in the analog to digital converters and demodulators that follow.

While the invention has been described according to what is presently considered to be the most practical and preferred embodiments, it must be understood that the invention is not limited to the disclosed embodiments. Those ordinarily skilled in the art will understand that various modifications and equivalent structures and functions may be made without departing from the spirit and scope of the invention as defined in the claims. Therefore, the invention as defined in the claims must be accorded the broadest possible interpretation so as to encompass all such modifications and equivalent structures and functions.

What is claimed is:

1. Apparatus for filtering and amplifying a received signal comprising:

a plurality of sequentially connected complex filter/amplifier stages, each stage having:

- complex filter means for attenuating an interfering portion relative to a desired portion of the received signal;
- controlled amplifier means having set minimum gain K_{min} and maximum gain K_{max} for amplifying the received signal; and
- control means for controlling the amplifier gain K where $K_{min} \leq K \leq K_{max}$ such that the controlled amplifier seeks to generate an output signal having a projected amplitude level.

2. Apparatus as claimed in claim 1wherein the received signal is in the IF band.

3. Apparatus as claimed in claim 2 wherein the received signal is at a low intermediate frequency (LIF).

4. Apparatus as claimed in claim 2 wherein the received signal is at a substantially zero intermediate frequency (ZIF).

5. Apparatus as claimed in claim 1 wherein the complex bandpass filter means filters the received signal and the amplifier means is connected to the filter means to amplify the filtered received signal.

6. Apparatus as claimed in claim 1 wherein the received signal comprises complex in-phase I and quadrature phase Q signals.

7. Apparatus as claimed in claim 6 wherein each of the complex filter means includes up to two poles.

8. Apparatus as claimed in claim 6 wherein the complex filter means comprises one or more single pole complex filters connected in series.

9. Apparatus as claimed in claim 6 wherein the controlled amplifier means comprises:

- a first variable gain amplifier for amplifying the in-phase I signal; and
- a second variable gain amplifier for amplifying the quadrature phase Q signal, wherein the control means generates a gain control signal for controlling the gain of the first and second amplifiers.

10. Apparatus as claimed in claim 9 wherein the control means determines the control signal as a function of the I and Q inputs to the amplifiers.

11. Apparatus as claimed in claim 9 wherein the control means determines the control signal as a function of the I and Q outputs of the amplifiers.

12. Apparatus as claimed in claim 9 wherein the control means determines the control signal as a function of the projected amplitude level.

13. Apparatus as claimed in claim 9 wherein the control means comprises:

- a first rectifier for receiving the output of the first variable amplifier to provide a first rectified signal;

- a second rectifier for receiving the output of the second variable amplifier to provide a second rectified signal;

- summing means for adding the first and the second rectified signals; and

- error amplifier means having a first input coupled to the summing means and a second input coupled to a projected amplitude level signal for producing the gain control signal.

14. Apparatus as claimed in claim 13 wherein the first and second rectifiers are full wave rectifiers.

15. Apparatus as claimed in claim 9 wherein the control means comprises:

- a first rectifier for receiving the input of the first variable amplifier to provide a first rectified signal;

- a second rectifier for receiving the input of the second variable amplifier to provide a second rectified signal;

- summing means to add the first and the second rectified signals; and

- error amplifier means having a first input coupled to the summing means and a second input coupled to a projected amplitude level signal for producing the gain control signal.

16. Apparatus as claimed in claim 15 wherein the first and second rectifiers are full wave rectifiers.

17. Apparatus as claimed in claim 9 further comprising:

received signal strength indicator having:

- gain summation means for receiving the gain control signal from each of the complex filter/amplifier stages for computing the overall gain of the apparatus;

- means for detecting the amplitude of the apparatus output signal; and

- means coupled to the gain summation means and the detector means for indicating the strength of a desired signal received by the apparatus.

18. Apparatus as claimed in claim 1 wherein each complex filter/amplifier stage further includes a dc compensation circuit for attenuating the dc offset of the received signal.

19. Apparatus as claimed in claim 18 wherein the dc compensation circuit is a feedback circuit.

20. Apparatus as claimed in claim 18 wherein the dc compensation circuit is a feedforward circuit.

21. Apparatus as claimed in claim 1 wherein K_{min} is negative.

Abstract

A low power IF strip architecture suitable for Zero-IF (ZIF) or low-IF (LIF) radio receivers for filtering and amplifying a received signal. The apparatus includes a plurality of sequentially connected complex filter/amplifier stages. Each stage includes a complex filter having one or more poles and an automatic gain controlled amplifier (AGC). Each AGC may be feedback or feedforward with fixed minimum and maximum gains. Each stage further includes a control circuit that produces a gain control signal for controlling the amplifier gain within the fixed minimum and maximum gains as a function of a projected amplitude level. The received signal passes through multiple stages of filtering and controlled amplification to attenuate the interfering signal and amplify the desired signal. This is done at a restricted level in each stage such that the circuits in the stages operate at efficient power saving levels. The individual gain control signals from each stage are summed in a received signal strength indicator to provide the overall gain of the apparatus. The overall gain when taken with the amplitude of the apparatus output signal determines the original strength of the desired received signal.

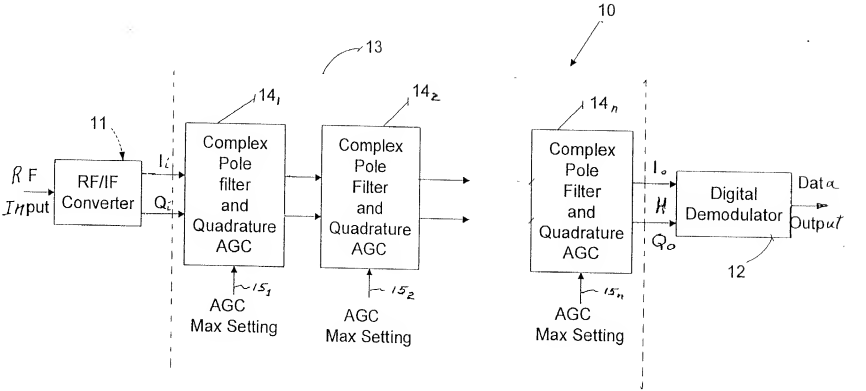

Figure 1

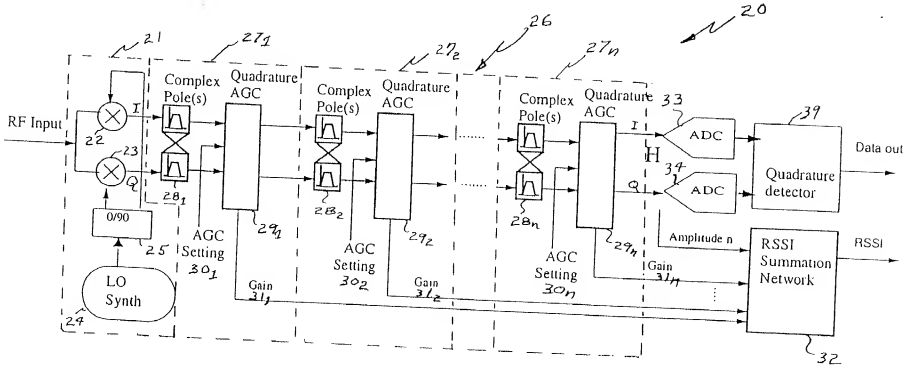

Figure 2

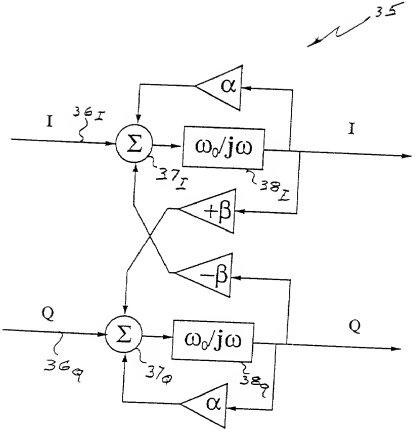

Figure 3

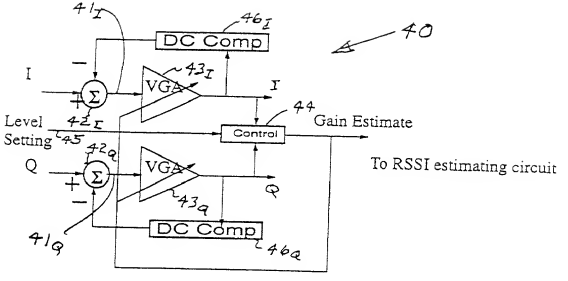

Figure 4a

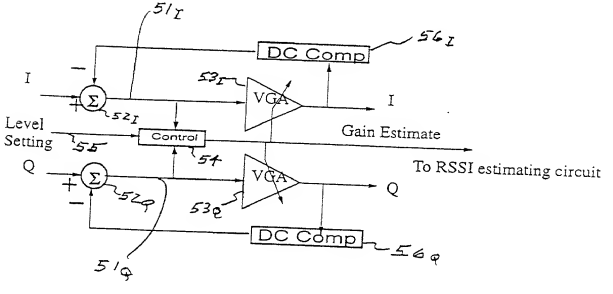

Figure 5a

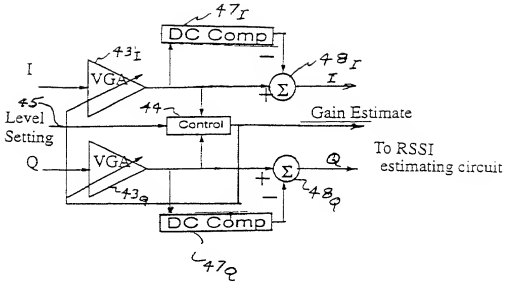

Figure 4b

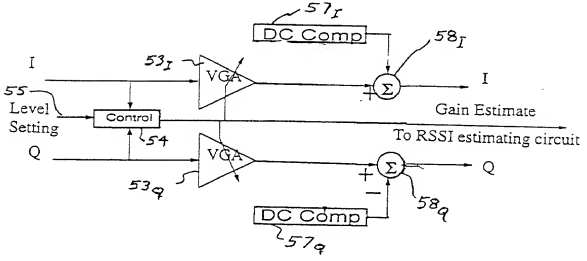

Figure 5b

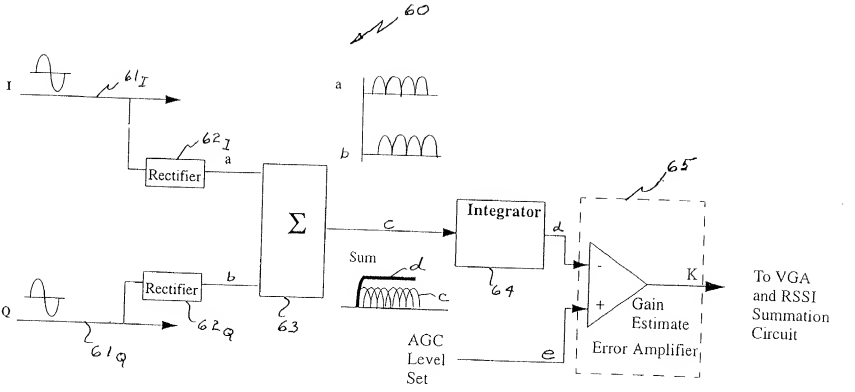

Figure 6

COMBINED DECLARATION AND POWER OF ATTORNEY
(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION, OR CIP)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is of the following type: (check one applicable item below)

☒ original
☐ design
☐ supplemental

NOTE: If the declaration is for an International Application being filed as a divisional, continuation or continuation-in-part application do not check next item, check appropriate one of last three items.

☐ national stage of PCT

NOTE: If one of the following 3 items apply then complete and also attach ADDED PAGES FOR DIVISIONAL, CONTINUATION OR CIP.

☐ divisional
☐ continuation
☐ continuation-in-part (CIP)

INVENTORSHIP IDENTIFICATION

WARNING: If the inventors are each not the inventors of all the claims an explanation of the facts, including the ownership of all the claims at the time the last claimed invention was made, should be submitted.

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

COMPLEX FILTERING/AGC RADIO RECEIVER ARCHITECTURE FOR LOW-IF OR ZERO-IF

SPECIFICATION IDENTIFICATION

the specification of which: (complete (a), (b) or (c))

(a) ☒ is attached hereto.

(b) ☐ was filed on [DATE] as Serial No._____; or
☐ was filed on [date], under Express Mail No. _____, as Serial No. not yet known, and was amended on _____(if applicable).

NOTE: Amendments filed after the original papers are deposited with the PTO which contain new matter are not accorded a filing date by being referred to in the declaration. Accordingly, the amendments involved are those filed with the application papers or, in the case of a supplemental declaration, are those amendments claiming matter not encompassed in the original statement of invention or claims. See 37 CFR 1.67.

(c) ☐ was described and claimed in PCT International Application No. _____; filed on _____ and as amended Under PCT Article 19 on _____ (if any).

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information

☒ which is material to patentability as defined in 37, Code of Federal Regulations, § 1.56;
(also check the following items, if desired)

☒ and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable examiner would consider it important in deciding whether to allow the application to issue as a patent; and

☐ In compliance with this duty, there is attached an information disclosure statement in accordance with 37 CFR 1.98.

PRIORITY CLAIM (35 U.S.C. § 119)

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

(complete (d) or (e))

(d) ☐ no such applications have been filed

(e) ☒ such applications have been filed as follows

NOTE: Where item (c) is entered above and the International Application which designated the U.S. claimed priority check item (e), enter the details below and make the priority claim.

A. PRIOR FOREIGN/PCT APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119

Country (or Indicate if PCT)	Application Number	Date of Filing (day/month/year)	Priority Claimed Under Section 37 USC 119
Canada	2,289,823	11/15/99	☒ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO

ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

1. ______________________________
2. ______________________________
3. ______________________________

NOTE: If the application filed more than 12 months from the filing date of this application is a PCT filing forming the basis for this application entering the United States as (1) the national stage, or (2) a continuation, divisional, or continuation-in-part, then also complete ADDED PAGES TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR DIVISIONAL, CONTINUATION OR CIP APPLICATION for benefit of the prior U.S. or PCT application(s) under 35 U.S.C. § 120.

POWER OF ATTORNEY

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (List name and registration number)

George M. Thomas, Reg. No. 22,260; James W. Kayden, Reg. No. 31,532; Scott A. Horstemeyer, Reg. No. 34,183; Stephen R. Risley, Reg. No. 35,659; Jeffrey R. Kuester, Reg. No. 34,367; Daniel J. Santos, Reg. No. 40,158; Daniel R. McClure, Reg. No. 38,962; Robert E. Stachler II, Reg. No. 36,934; David P. Kelley, Reg. No. 17,420; Reg. No. 41,344; David R. Risley, Reg. No. 39,345; Jon E. Holland, Reg. No. 41,077; Dan R. Gresham, Reg. No 41,805; J. Scott Culpepper, Reg. No. 41,692; M. Paul Qualey, Reg. No 43,024; Robert P. Biddle, Reg. No. 35,826; Robert A. Blaha, Reg. No. 43,502; Jennifer M. Gruber, Reg. No. 42,601; Raymond W. Armentrout, Reg. No. 45,866; Cynthia J. Lee, Reg. No. 46,033; N. Andrew Crain, Reg. No. 45,442; Monica A. Hyson, Reg. No. P46,790; Sami O. Malas, Reg. No. 44,893; Marianne H. Parker, Reg. No. 46,169

(check the following item, if applicable)

☐ Attached as part of this declaration and power of attorney is the authorization of the above-named attorney(s) to accept and follow instructions from my representative(s).

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DIRECT TELEPHONE CALLS TO:

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DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

NOTE: Carefully indicate the family (or last) name as it should appear on the filing receipt and all other documents

Full name of sole or first inventor

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CHECK PROPER BOX(ES) FOR ANY OF THE FOLLOWING ADDED PAGE(S) WHICH FORM A PART OF THIS DECLARATION

☐ Signature for subsequent joint inventors. Number of pages added ______.

* * *

☐ Signature by administrator(trix), executor(trix) or legal representative for deceased or incapacitated inventor. Number of pages added ______.

* * *

☐ Signature for inventor who refuses to sign or cannot be reached by person authorized under 37 CFR 1.47. Number of pages added ______.

* * *

☐ Added pages to combined declaration and power of attorney for divisional, continuation, or continuation-in-part (CIP) application.

☐ Number of pages added ______

* * *

☐ Authorization of attorney(s) to accept and follow instructions from representative.

* * *

If no further pages form a part of this Declaration then end this Declaration with this page and check the following item

☒ **This declaration ends with this page**

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